

1 2. (amended) The read/write amplifier as claimed in claim 1, wherein the amplifier
2 components have at least one N latch circuit for amplifying a voltage signal to a low level and/or
3 at least one P latch circuit for amplifying a voltage signal to a high level and/or at least one
4 equalizer for producing a reference voltage value on the bit line(s) and the reference bit line(s)
5 and/or at least one bit switch for connecting at least one selected bit line pair to at least one
6 external data line.

1 3. (amended) The read/write amplifier as claimed in claim 2, wherein at least one N
2 latch circuit and at least one P latch circuit are provided in the first read/write amplifier element.

1 4. (amended) The read/write amplifier as claimed in claim 2, wherein at least one
2 equalizer is provided in the first read/write amplifier element.

1 5. (amended) The read/write amplifier as claimed in claim 2, wherein at least one N
2 latch circuit is provided in the second read/write amplifier element.

1 6. (amended) The read/write amplifier as claimed in claim 2, wherein at least one bit
2 switch is provided in the second read/write amplifier element.

1 7. (amended) The read/write amplifier as claimed in claim 1, wherein the second
2 read/write amplifier element is connected or can be connected to at least one external data line.

1 8. (amended) The read/write amplifier as claimed in claim 1, wherein the second
2 read/write amplifier element is connected or can be connected to at least one further read/write
3 amplifier.

1 9. (amended) The read/write amplifier as claimed in claim 1, wherein the first and/or
2 second read/write amplifier element(s) has/have one or more transistors for changing over
3 between different bit lines and reference bit lines, respectively.

1 10. (amended) A DRAM memory, having a number of DRAM memory cells, which
2 each form one or more memory cell arrays, each memory cell being connected to a bit line and
3 the bit lines furthermore being connected to at least one read/write amplifier, wherein the at least
4 one read/write amplifier is designed as a read/write amplifier as claimed in claim 1.

1 11. (amended) The DRAM memory as claimed in claim 10, wherein at least one word
2 line is provided, which is routed across the memory cell array(s) and, for activation of the
3 DRAM memory cells, is connected to one or more memory cell(s).

1 12. (amended) The DRAM memory as claimed in claim 10, wherein a plurality of bit
2 lines of a memory cell array are connected to a read/write amplifier.

1 13. (amended) The DRAM memory as claimed in claim 10, wherein in each case a bit
2 line of a DRAM memory cell that is to be evaluated and a reference bit line of a DRAM memory
3 cell that is not to be evaluated form a bit line pair, and in that each bit line pair is connected both
4 to the first and to the second read/write amplifier element.

1 14. (amended) The DRAM memory as claimed in claim 10, wherein the connection
2 of a bit line and/or reference bit line to a read/write amplifier is activated or can be activated via
3 one or more transistors.

- 1 15. (amended) A method for evaluating DRAM memory cells of a DRAM memory,
2 in particular of a DRAM memory as claimed in claim 10, and in particular using a read/write
3 amplifier as claimed in claim 1, having the following steps:
4 a) activation of one or more memory cells that are to be evaluated via at least one word
5 line;
6 b) activation of a connection of at least one first bit line pair, formed from a bit line of the
7 memory cell that is to be evaluated and a reference bit line of a memory cell that is not to be
8 evaluated, to a first read/write amplifier element, and activation of the connection of at least one
9 second bit line pair, adjacent to the first bit line pair, to a second read/write amplifier element,
10 the two bit line pairs in each case being connected to the first and second read/write amplifier
11 elements;
12 c) amplification of the voltage signals read out via the first bit line pair by means of at
13 least one N latch circuit provided in the first read/write amplifier element and also a P latch
14 circuit, and amplification of the voltage signals read out via the second bit line pair by means of
15 at least one N latch circuit provided in the second read/write amplifier element;
16 d) evaluation and writing back of the data of the memory cell(s) that is/are to be
17 evaluated and is/are actively connected to the first read/write amplifier element;
18 e) changeover of the connection between the bit line pairs and the first read/write
19 amplifier element in such a way that the P latch circuit of the first read/write amplifier element is
20 changed over to the second read/write amplifier element;
21 f) evaluation and writing back of the data of the memory cell(s) that is/arc to be evaluated
22 and is/are actively connected to the second read/write amplifier element; and
23 g) deactivation of the memory cells that are to be evaluated.

- 1 17. (amended) The method as claimed in claim 15, wherein the bit line pair which is
2 actively connected to the first read/write amplifier element is disconnected from the first
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- 1 read/write amplifier element after the end of step d), with the result that the bit line and the
- 2 reference bit line float with full voltage levels, and in that the N latch circuit of the first
- 3 read/write amplifier element is subsequently switched off.

- 1 18. (amended) The method as claimed in claim 15, wherein, after the activation of a
- 2 bit switch provided in the second read/write amplifier element, a voltage difference is generated
- 3 on one or more external data line(s) connected to said bit switch.

- 1 19. (amended) The method as claimed in claim 15, wherein, after the end of the
- 2 evaluation operation, the uniform reference voltage is applied to all the bit lines of the evaluated
- 3 memory cells via an equalizer.